



MICROCHIP

PIC18F2480/2580/4480/4580

PIC18F2480/2580/4480/4580 Rev. B0 Silicon Errata

The PIC18F2480/2580/4480/4580 Rev. B0 parts you have received conform functionally to the Device Data Sheet (DS39637C), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2480/2580/4480/4580 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F2480/2580/4480/4580 silicon.

The following silicon errata apply only to PIC18F2480/2580/4480/4580 devices with these Device/Revision IDs:

| Part Number | Device ID | Revision ID |
|-------------|---------------|-------------|
| PIC18F2480 | 0001 1010 100 | 0 0010 |
| PIC18F2580 | 0001 1010 110 | 0 0010 |
| PIC18F4480 | 0001 1010 101 | 0 0010 |
| PIC18F4580 | 0001 1010 100 | 0 0010 |

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: Master Synchronous Serial Port (MSSP)

When configured for I²C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.
This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

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2. Module: Brown-out Reset (BOR)

The BOR module may reset above the parameter D005 value specified in Section 27.1 DC Characteristics: Supply Voltage when:

- BORV<1:0> = 01 or 00
- FOSC is above 26 MHz

The updated BOR voltage specifications are shown.

27.1 DC Characteristics: Supply Voltage PIC18F2480/2580/4480/4580 (Industrial, Extended) PIC18LF2480/2580/4480/4580 (Industrial)

| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
|-----------|--------|--------------------------------|------|------|------|-------|---------------|
| D005 | VBOR | Brown-out Reset Voltage | | | | | |
| | | BORV1:BORV0 = 01 | 4.47 | 4.69 | 4.91 | V | Fosc > 26 MHz |
| | | BORV1:BORV0 = 00 | 4.72 | 4.95 | 5.18 | V | Fosc > 26 MHz |

Work around

To address this situation:

- Reduce FOSC to 25 MHz
- Use the lower of the two affected BOR voltage thresholds, BORV<1:0> (CONFIG2L<4:3>) = 01

This will ensure detection of VDD below 5.0V.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (10/2008)

Original version of this document. Includes silicon issue 1 (Master Synchronous Serial Port – MSSP).

Rev B Document (3/2009)

Added silicon issue 2 (BOR).

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NOTES:

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